REMARKS

I. Introduction

In response to the pending Office Action, Applicants have amended Figs. 46 and 47 to include the legend "Prior Art". The specification has been amended such that the description of the drawings accurately identifies the figures contained in the specification. In addition, claim 1 has been amended to clarify the intended subject matter of the invention. No new matter has been added.

Applicants also note that an Information Disclosure Statement (IDS) was filed in the above-identified application on January 17, 2002. Applicants respectfully request that the Examiner initial and return the PTO-1449 form which was filed along with the IDS so that the Applicants can confirm that the references have been considered. If for any reason the Examiner has not received the IDS, the Examiner is respectfully requested to contact the undersigned attorney so that another copy of the IDS can be provided to the Examiner.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. Objection To The Drawings

In paragraph 3 of the Office Action, the drawings were objected to for failing to show every feature of the invention recited by the claims. In particular, the Examiner based the objection on the failure to illustrate "an equivalent circuit" and "analysis control information". Applicants respectfully submit that the foregoing objection is

improper. The pending claims are **method** claims directed to a process of estimating electromagnetic interference of an LSI. Both of the terms set forth above refer to data generated and/or utilized during the estimation process. Neither term represents a structural element in a device. As such, it is respectfully submitted that there is no requirement that these elements be illustrated in the drawings. The figures submitted with the application provide numerous flow charts that clearly set forth the process of the present invention when read in light of the specification.

Based on the foregoing, it is respectfully requested that the foregoing objection to the drawings be withdrawn.

III. The Rejection Of The Claims Under 35 U.S.C. § 112

Claims 1-10 were rejected 35 U.S.C. § 112, second paragraph, for failing to particularly point out and claim the subject matter of the invention. Specifically, the rejection stated that the "the circuit information of said LSI chip" was unclear and not supported by the specification, and that the phrase "an equivalent circuit" was unclear and not supported by the specification. Applicants respectfully traverse the pending rejection for the following reasons.

First, with regard to "circuit information of the LSI chip", Applicants wish to direct the Examiner's attention to page 24 lines 5-18, which provides an example of the circuit information recited by claim 1 and utilized in the claimed estimation process. As noted therein, "circuit information" corresponds to connection information among one or more circuit elements, lines and external terminals, and information of the current when each of the circuit elements is driven. Fig. 3 illustrates an example of such circuit

information. Based on the foregoing, it is respectfully submitted that the circuit information of the LSI chip is clearly defined by the originally filed specification, and would be readily understood by those of skill in the art.

With regard to the question raised in the rejection of whether an equivalent power source current is the same as the power source current, the equivalent power source current corresponds to a model of an equivalent power source which simplifies the calculations performed during the simulation. The model represents the current flowing in the power source current, which corresponds to the actual circuit, which is not modeled.

Finally, with regard to the recited "equivalent circuit", as expressly recited on page 9, lines 3-11 of the specification, the equivalent circuit represents the combination of the: (1) circuit information and the (2) analysis information, where the analysis information includes at least one of power source information of a power source for supplying a current to the LSI, package information of the LSI and measurement system information of a measurement system for measuring characteristics of the chip. The combination of the circuit information and the analysis information is referred to as the total information, which is utilized to define the equivalent circuit.

In view of the foregoing, it is respectfully submitted that each of the terms identified in the pending rejection are fully supported by the specification, and would be readily understandable by those of skill in the art. As such, it is respectfully requested that the pending rejection be withdrawn.

IV. The Rejection Of The Claims Under 35 U.S.C. § 102

Claims 1-10 were rejected under 35 U.S.C. § 102 as being anticipated by USP No. 6,281,697 to Masuda. Applicants respectfully traverse the pending rejection for the reasons set forth below.

As recited by claim 1, the present invention relates to a method of estimating electromagnetic interference of an LSI. In the first step of the novel process, equivalent power source current information corresponding to the actual power source current is calculated from the circuit information of the LSI. In the second step of the claimed process, which is an estimating step, at least one of power source information of a power source for supplying a current to the LSI; package information of the LSI; and measurement system information of a measurement system for measuring characteristics of the chip is reflected in the circuit information of the LSI to estimate an equivalent circuit. In other words, the combination of the circuit information and the analysis information, which is referred to as the total information, is utilized to define the equivalent circuit.

Turning to Masuda, it is respectfully submitted that, at a minimum, Masuda fails to disclose either of the foregoing steps of the claimed invention.

First, with regard to claim 1, Masuda does not disclose an equivalent power source calculating step. As noted above, the claimed equivalent power source current corresponds to a model of an equivalent power source which simplifies the calculations performed during the simulation. The model represents the current flowing in the power source current, which is the actual power source current. In contrast, in Masuda, there is no modeling of the power source current of the LSI circuit. Masuda simply discloses

measuring the current passing through a printed wires disposed on a test board. There is no modeling or calculation of an equivalent of the power supply module 307 of Masuda. Thus, Masuda fails to disclose this element of claim 1.

Second, as noted, the claimed estimating step recites that at least one of power source information of a power source for supplying a current to the LSI; package information of the LSI; and measurement system information of a measurement system for measuring characteristics of the chip is reflected in the circuit information of the LSI to estimate the total information of an equivalent circuit. In contrast, Masuda does not perform any of the foregoing steps. As expressly noted in Masuda, the actual current flowing the printed wires 303 is determined by measuring the magnetic field surrounding the printed wires. However, the conversion tables of Masuda for converting the magnetic field to current values do not consider at least one of power source information of a power source for supplying a current to the LSI; package information of the LSI; and measurement system information of a measurement system for measuring characteristics of the chip is reflected in the circuit information of the LSI. Thus, Masuda also fails to disclose this limitation.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, ***Kalman v. Kimberly-Clark Corp.***, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), and Masuda fails to disclose at least the foregoing steps of the process recited by claim 1 of the present invention, it is clear that Masuda does not anticipate claim 1, or any claim dependent thereon.

For the foregoing reasons, it is respectfully submitted that claim 1, and all claims dependent thereon, are patentable over Masuda.

V. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.***, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all pending dependent claims are also in condition for allowance.

Further, it is respectfully submitted that claims 11-25 be rejoined in this application, as each of these claims is dependent on claim 1, and claim 1 is allowable for the reasons set forth above, it is clear that claim 1 represents a generic claim with respect to claims 11-25.

VI. Request For Notice Of Allowance

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an

Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

McDERMOTT, WILL & EMERY

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